



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/899,093	07/06/2001	Michael O. Thompson	3672-0121P	2736

2292 7590 05/08/2002

BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

EXAMINER

HUR, JUNG H

ART UNIT	PAPER NUMBER
----------	--------------

2824

DATE MAILED: 05/08/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/899,093

Applicant(s)

THOMPSON ET AL.

Examiner

Jung (John) Hur

Art Unit

2824

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on July 6, 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on ____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☒ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) ____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☒ Other: search history.

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Norway on July 7, 2000. It is noted, however, that applicant has not filed a certified copy of the 20003508 application as required by 35 U.S.C. 119(b).

Preliminary Amendment

2. Acknowledgment is made of applicant's preliminary amendment to claim 8.

Information Disclosure Statement

3. The listing of references in the specification is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609 A(1) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered.

Drawings

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference signs not mentioned in the description: "V_{switch}" and "P_s" in Fig. 1; "0" through "12" in Figs. 6, 7, and 9-14; and "0" through "11" in Fig. 8. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference signs in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Art Unit: 2824

5. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: "E_c" on page 3, line 9; "PR" on page 10, line 14; "V_s" on page 10, line 22; time markers, for example, t₀ through t₁₂ on page 15; and "V_{READ}" on page 23, line 27. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

6. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because, in Fig. 8, reference character "9" has been used to designate both 9th and 10th time markers. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

7. The spacing of the lines of the specification is such as to make reading and entry of amendments difficult. New application papers with lines double spaced on good quality paper are required.

8. The disclosure is objected to because of the following informalities: on page 3, line 22, "discloses" should be --discloses--; figure references for the time markers "t₀" through "t₄" and "t₆" on pages 16 and 17 appear to be inconsistent with the descriptions; figure references on page 17, lines 24 and 25 appear to be inconsistent with the descriptions; and description for "t₈" on page 17 appears to be improper. Appropriate correction is required.

9. Claims 1-16 are objected to because of the following informalities: claim 1 uses the terms "read cycle" and "refresh/write cycle" with quotation marks, while claims 2 and 13-16 use

Art Unit: 2824

said terms without quotation marks, claims 3-5 use the term "read, refresh and write cycles" without quotation marks, claim 6 uses the term "read/write cycle" without quotation marks, claim 9 uses the term "read/write protocol" without quotation marks, and claim 11 uses "read/refresh/write cycle protocols" without quotation marks; in describing addressed and non-addressed cells, word lines and bit lines, claims 1, 9 and 13 use the terms "selected" and "non-selected", while claims 3-7, 12 and 15 use the terms "addressed" and "non-addressed", and claims 9, 14 and 15 use the terms "active" and "inactive"; and other similar informalities. Appropriate correction is required.

10. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

11. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

12. Claims 1-16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claims are generally narrative and indefinite, failing to conform with current U.S. practice. They appear to be a literal translation into English from a foreign document and are replete with grammatical and idiomatic errors.

There is insufficient antecedent basis for the following limitations in the claims:

claim 1 recites the limitation "said matrix" in line 6 of the claim;

Art Unit: 2824

claim 1 recites the limitation "said n potentials" in lines 10 and 11 of the claim;

claim 1 recites the limitation "the charges" in line 17 of the claim;

claim 1 recites the limitations "the bit line(s)", "the cells", and "said bit line(s)" in line 18 of the claim;

claim 1 recites the limitation "said selected bit line(s)", "the cells", and "said bit line(s)" in lines 21 and 22 of the claim;

claim 2 recites the limitation "the bit line" in line 3 of the claim;

claim 2 recites the limitation "said read cycle" in line 4 of the claim;

claim 2 recites the limitation "the refresh/write cycle" in line 5 of the claim;

claim 3 recites the limitation "the voltages across non-addresses cells" in line 3 of the claim;

claim 3 recites the limitation "the voltage across the addressed cell" in line 4 of the claim;

claim 4 recites the limitation "the voltages across non-addresses cells" in line 3 of the claim;

claim 4 recites the limitation "the voltage across the addressed cell" in line 4 of the claim;

claim 5 recites the limitation "the voltages across non-addresses cells" in line 3 of the claim;

claim 5 recites the limitation "the voltage across the addressed cell" in line 4 of the claim;

claim 6 recites the limitation "the read/write cycle" in line 3 of the claim;

claim 6 recites the limitation "the exact values $V_s/2$ or $V_s/3$ " in line 4 of the claim;

claim 7 recites the limitation "the exact values $V_s/2$ or $V_s/3$ " in lines 3 and 6 of the claim;

Art Unit: 2824

claim 9 recites the limitation “the potentials Φ_{inactive} WL of inactive word lines” in lines 2 and 3 of the claim;

claim 9 recites the limitation “the potentials Φ_{inactive} BL of inactive word lines” in lines 4 of the claim;

claim 9 recites the limitation “the read/write protocols” in line 5 of the claim;

claim 11 recites the limitation “the read/refresh/write cycle protocol” in lines 3 and 4 of the claim;

claim 13 recites the limitation “the selected bit line(s)” in line 2 of the claim;

claim 13 recites the limitation “the bit line” in line 6 of the claim;

claim 14 recites the limitation “the read cycle” in lines 2 and 5 of the claim;

claim 14 recites the limitation “the non-addressed cells” and “said non-addressed cells” in lines 3 and 8 of the claim;

claim 14 recites the limitation “the active bit lines” in line 11 of the claim;

claim 15 recites the limitation “the read cycle” and “said read cycle” in lines 2, 3 and 4 of the claim;

claim 15 recites the limitation “the pulse protocol and current detection” in line 4 of the claim;

claim 15 recites the limitation “the circuitry” in line 7 of the claim;

claim 15 recites the limitation “the logic state of the addressed cell” in lines 7 and 8 of the claim;

claim 16 recites the limitation “said signal” in line 2 of the claim;

claim 16 recites the limitation “the pre-read cycle” in line 2 of the claim; and

Art Unit: 2824

claim 16 recites the limitation "the read cycle" in line 3 of the claim.

Claim Rejections - 35 USC § 102

13. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

14. Claims 1-3 and 11-14, insofar as understood, are rejected under 35 U.S.C. 102(b) as being anticipated by Kuroda (U.S. Pat. No. 5,550,770).

Regarding claims 1-3, Kuroda discloses, in Figs. 1-15 and respective portions of the specification, a memory array of cells comprising ferroelectric capacitors and a method of driving said memory array of cells, wherein all word lines and bit lines (data lines, in the reference) are controlled with a plurality of pre-defined potential levels in a predetermined, time-coordinated sequence. Kuroda further discloses read, refresh (rewrite, in the reference) and write cycles in the predetermined, time-coordinated sequence; during the read cycle, potential on a selected bit line floats in response to flowing charges when the charges are sensed (Fig. 15), and during the write or refresh cycle, the word line and bit line potentials are clamped to said sequence of potentials (Figs. 12-14). Kuroda further discloses, in Figs. 9, 10 and 12-15, three potential levels for word lines and bit lines (data lines, in the reference), such that voltage across unselected cells is about $V_s/2$ ($V_0/2$, in the reference), where V_s is defined on page 10, lines 20-27 in the instant specification.

Regarding claims 11-14, Kuroda discloses same quiescent potentials on all the word lines and bit lines (data lines, in the reference), namely, $V_0/2$ in Figs. 9 and 10, and 0 V in Figs. 12-15,

Art Unit: 2824

where $V_0/2$ is same as the potential on unselected word lines and bit lines, and 0 V represents system ground (Figs. 2-8). In Fig. 10(C), Kuroda further discloses a precharge period where the potential on a selected bit line is changed from a quiescent potential before a floating period in which the flowing charge is sensed (precharge of data line and sense steps, in the reference). In Fig. 15, Kuroda further discloses a precharge pulse on unselected word lines as an option, such that said precharge pulse terminates when the potential on a selected bit line changes for a read cycle. With the precharge pulse, the voltage across unselected cells on the selected bit line would be about $V_0/2$ from the onset of the precharge pulse until the read cycle is completed.

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

16. Claims 4 and 6-10, insofar as understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroda (U.S. Pat. No. 5,550,770) in view of Tannas (U.S. Pat. No. 4,169,258).

Regarding claim 4, Kuroda discloses a method of driving a ferroelectric memory array as in claim 1 (see above). However, Kuroda does not disclose four (4) potential levels for word lines and bit lines. Tannas discloses, in Figs. 3a-3d, four potential levels for driving a ferroelectric matrix, such that the voltage across unselected cells do not significantly exceed $V_s/3$, for the purpose of minimizing hysteresis creep and preventing undesirable hysteresis switching. Therefore, in view of Tannas, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method of Kuroda to

Art Unit: 2824

use four potential levels of Tannas for the purpose of minimizing hysteresis creep and preventing undesirable hysteresis switching.

Regarding claims 6-10, Kuroda discloses a method of driving a ferroelectric memory array as in claim 1 (see above). Kuroda further discloses that the voltage across unselected cells is about one half of applied voltage across a selected cell. However, Kuroda does not disclose details of any deviation of voltages across unselected cells nor details of any deviation of potentials on word lines and bit lines. Tannas, in the specification, discloses that potentials on word lines (x-lines, in the reference) and bit lines (y-lines, in the reference) may shift either negatively or positively. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to increase the voltage across unselected cells along a selected word line by a controlled voltage and to decrease the voltage across unselected cells along a selected bit line by the same controlled voltage, or to increase the potential of unselected word lines by a controlled voltage and to decrease the potential of unselected bit lines by the same controlled voltage, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum value of a result effective variable involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

17. Claim 5, insofar as understood, is rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroda (U.S. Pat. No. 5,550,770) in view of Anderson (U.S. Pat. No. 3,002,182).

Regarding claim 5, Kuroda discloses a method of driving a ferroelectric memory array as in claim 1 (see above). However, Kuroda does not disclose five potential levels, of which any set of three are for word lines and any other set of three are for bit lines. Anderson discloses, in Fig. 4, for the purpose of reducing the effect of disturbing pulses on unselected cells, three

Art Unit: 2824

potential levels for word lines (rows, in the reference) and three potential levels for bit lines (columns, in the reference) with a total of five distinct potential levels for operating a ferroelectric matrix, such that the voltage across unselected cells do not significantly exceed $V_s/3$. Therefore, in view of Anderson, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method of Kuroda to use five potentials levels of Anderson for the purpose of reducing the effect of disturbing pulses on unselected cells.

Allowable Subject Matter

18. Claims 15 and 16, insofar as understood, would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The prior arts of record do not disclose or suggest a method of applying a pre-read reference cycle which precedes a read cycle by a selected time, wherein a signal obtained during the pre-read reference cycle is subtracted from a signal obtained during the read cycle.

Conclusion

19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Anderson (U.S. Pat. No. 2,972,734) discloses a method of applying compensating pulses in addition to read pulses for the purpose of reducing noise in read signals.

Application/Control Number: 09/899,093

Art Unit: 2824

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jung (John) Hur whose telephone number is (703) 308-1624.

The examiner can normally be reached on M-F 6:00 AM - 2:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (703) 308-2816. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

jhh
May 6, 2002



RICHARD ELMS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800